(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 1 345 275 A1

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
17.09.2003 Bulletin 2003/38

(51) Int Cl.7: **H01L 33/00**, H01L 21/308, H01L 21/033

(21) Application number: **02100242.3**

(22) Date of filing: **13.03.2002**

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE TR
Designated Extension States:
AL LT LV MK RO SI

(71) Applicants:
- **Sakai, Shiro**
  Tokushima 770-8072 (JP)
- **Nitride Semiconductors Co., Ltd.**
  Naruto-shi, Tokushima 771-0360 (JP)

(72) Inventors:
- **Sakai, Shiro**
  770-8072, Tokushima (JP)
- **Lacroix, Yves**
  770-0855, Tokushima (JP)

(74) Representative: **Weihs, Bruno**
Rosenthal & Osha S.A.R.L.
121, avenue des Champs Elysées
75008 Paris (FR)

(54) Method for roughening semiconductor surface

(57) In order to provide a method for easily roughening a surface of a semiconductor constituting an LED, a first material 18 and a second material 20 having a property that they are nonuniformly mixed when thermally treated are deposited on a semiconductor 16, the structure is thermally treated, and etching is performed through reactive ion etching in which the etching rate with respect to the first material 18 is slower than the etching rates with respect to the second material 20 and to the semiconductor 16. During this process, a region 22 in which the first material 18 is the primary constituent functions as an etching mask, and a predetermined roughness can be easily formed on the surface of the semiconductor 16.

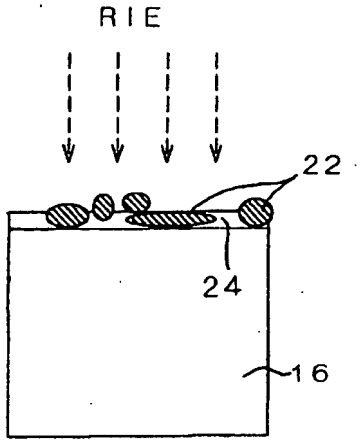

FIG. 2(c)

EP 1 345 275 A1

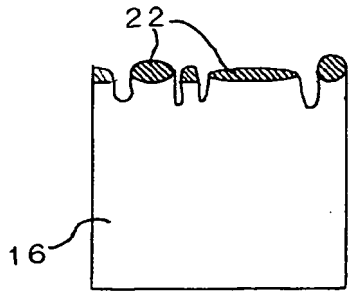

FIG. 2(d)

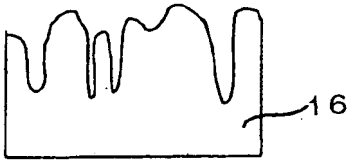

FIG. 2(e)

Description

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] The present invention relates to an improvement in a method for roughening a surface of a semiconductor, in particular, a gallium nitride semiconductor.

2. Description of the Related Art

[0002] In a light emitting diode (LED), a PN junction 14 formed from an N type layer 10 and a P type layer 12 is used as the light emitting section, as shown in Fig. 1(a). The light emitted from the light emitting section is extracted for use in various applications. In such an LED, the surface of the element is usually formed flat. When the surface of the LED is flat, a large portion of the light emitted from the PN junction 14 is reflected at the surface of the LED, as shown in Fig. 1(a), and is not emitted to the outside. Because of this, there had been a problem in that the light extraction efficiency cannot be increased.

[0003] In order to solve this problem, it is effective to roughen the surface for extracting light of the semiconductor which constitutes the LED, as shown in Fig. 1 (b) . When a surface of the semiconductor constituting the LED is roughened, reflection, at the light extraction surface of the semiconductor, of the light generated at the PN junction 14 back to the inside of LED when the light reaches the light extraction surface can be avoided, as shown in Fig. 1(b). This facilitates extraction of light to the outside of the LED and the light extraction efficiency of the LED can be improved.

[0004] Moreover, when the surface of the semiconductor constituting the LED is roughened, the surface area is significantly increased compared to a flat surface. This facilitates ohmic contact and thus, formation of an electrode.

[0005] However, conventionally, there had been no method for easily roughening the surface of the semiconductor constituting the LED.

SUMMARY OF THE INVENTION

[0006] The present invention was conceived to solve the above problem and one object of the present invention is to provide a method for easily roughening a surface of a semiconductor constituting an LED.

[0007] In order to achieve at least the object mentioned above, according to the present invention, there is provided a method for roughening a surface of a semiconductor comprising the steps of depositing, on a surface of a semiconductor, a first material and a second material having a property that when thermally treated, the first and second materials are nonuniformly mixed; thermally treating the semiconductor onto which the two materials are deposited; and etching the surface of the semiconductor onto which the two materials are deposited through an etching method in which the etching rate of the first material is slower than the etching rates of the second material and of the material for the semiconductor.

[0008] According to another aspect of the present invention, it is preferable that in the method for roughening the surface of a semiconductor, the first and second materials are evaporated as layers onto the surface of the semiconductor through vacuum evaporation.

[0009] According to another aspect of the present invention, it is preferable that in the method for roughening the surface of a semiconductor, the semiconductor is a gallium nitride semiconductor, the first material is Ni, the second material is Au, and the etching method is reactive ion etching.

[0010] With the above structures, two materials deposited on the semiconductor surface are nonuniformly mixed, and because the etching rate of the first material is slower than the etching rates of the second material and of the semiconductor, the first material functions as an etching mask so that unevenness can be created on the semiconductor surface.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011]

Figs. 1 (a) and 1 (b) are diagrams for explaining how the light is extracted from a light emitting diode in the prior art.

Figs. 2 (a) ~ 2 (e) are diagrams for explaining the steps for a method for roughening a surface of a semiconductor according to the present invention.

Fig. 3 (a) is a diagram showing the relationship between the ratio of etching rates of GaN and Ni and plasma power.

Fig. 3(b) is a diagram showing the relationship between the surface roughness and plasma power.

DESCRIPTION OF PREFERRED EMBODIMENT

[0012] A preferred embodiment of the present invention will now be described referring to the drawings.

[0013] Figs. 2 (a) through 2 (e) show the steps for a method for roughening a surface of a semiconductor according to the present invention. As shown in Fig. 2 (a), a first material 18 and a second material 20 are deposited on a surface of a semiconductor 16 which constitutes an LED. The first material 18 and second material 20 are materials that have a property such that when these materials are thermally treated, they melt into each other to form a nonuniform mixture state. For example, when nickel (Ni) is used as the first material 18 and gold (Au) is used as the second material 20, the materials mix with each other when thermally treated, but the mixing is nonuniform. Because of this, by ther-

mally treating the semiconductor 16 onto which the two materials 18 and 20 are deposited, a region 22 where the composition of Ni which is the first material 18 is large can be formed as spots in a region 24 where the composition of Au which is the second material 20 is large.

[0014] In order to deposit the first material 18 and the second material 20 on the surface of the semiconductor 16, for example, vacuum evaporation can be employed to deposit the first material 18 and the second material 20 as layers on the surface of the semiconductor 16. However, the method for depositing the two materials 18 and 20 is not limited to the above vacuum evaporation and any deposition method can be employed that allows the first material and the second material to nonuniformly mix when the structure is thermally treated.

[0015] Next, as shown in Fig. 2 (c), the surface of the semiconductor 16 onto which the first material 18 and the second material 20 are deposited is etched through an etching method in which the etching rate of the first material 18 is slower than the etching rates of the second material 20 and of the semiconductor 16. For example, when Ni is used as the first material 18, Au is used as the second material 20, and gallium nitride (GaN) is used as the material for the semiconductor 16 as described above, reactive ion etching (RIE) can be employed as the etching method in order to selectively etch as above.

[0016] Fig. 3 (a) shows the relationship between a ratio of the etching rates of GaN and Ni and the plasma power to be applied, when the structure is etched in an RIE device. Fig. 3 (b) shows the relationship between the roughness of the surface of the semiconductor (GaN) and the plasma power in such a case. As is clear from Figs. 3 (a) and 3 (b), when the applied plasma power is small, GaN is selectively etched and Ni is not etched, and therefore, the surface roughness of GaN is high. Although not shown in the figures, the etching rate in RIE of Au which is the second material is larger than those of GaN and Ni.

[0017] In this manner, when the above combination of materials are used and RIE is employed as the etching method, Ni which is the primary constituent of the region 22 where the composition of the first material is large functions as an etching mask, and Au which is the primary constituent of the region 24 where the composition of the second material is large and GaN which is the material for the semiconductor 16 are selectively etched, as shown in Fig. 2 (d). Therefore, if the etching process is performed for a predetermined period of time, a predetermined unevenness of the surface of GaN which is the material for the semiconductor 16 is formed, as shown in Fig. 2 (e).

[0018] In the above discussion, Ni is used as the first material 18 and Au is used as the second material 20, but the materials are not limited to these. In other words, any combination of materials can be used as long as the etching rates for RIE differ significantly and the materials can be nonuniformly mixed by thermal treatment.

As described, according to the present invention, two materials that mix nonuniformly when thermally treated are deposited on a surface of a semiconductor, the structure is thermally treated, and then etching process is performed by a method which can selectively etch one of the materials and the semiconductor. Through this process, the surface of the semiconductor can easily be roughened.

Claims

1. A method for roughening a surface of a semiconductor comprising the steps of:

   depositing, on a surface of a semiconductor, a first material and a second material having a property that when thermally treated, the first and second materials are nonuniformly mixed;
   thermally treating the semiconductor onto which the two materials are deposited; and
   etching the surface of the semiconductor onto which the two materials are deposited through an etching method in which the etching rate of the first material is slower than the etching rates of the second material and of the material for the semiconductor.

2. A method for roughening a surface of a semiconductor according to claim 1, wherein the first and second materials are evaporated as layers onto the surface of the semiconductor through vacuum evaporation.

3. A method for roughening a surface of a semiconductor according to claim 1, wherein the semiconductor is a gallium nitride semiconductor, the first material is Ni, the second material is Au, and the etching method is reactive ion etching.

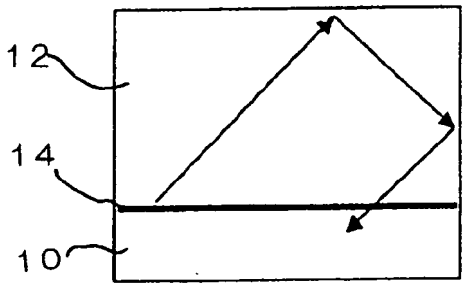

FIG. 1(a)

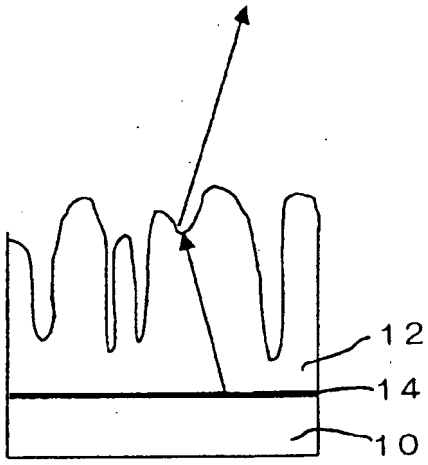

FIG. 1(b)

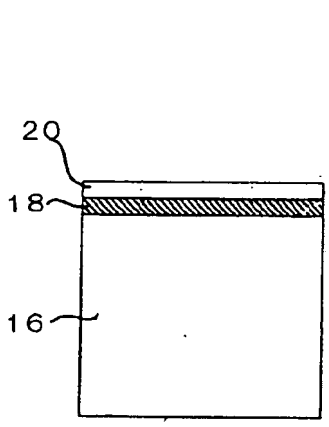

FIG. 2(a)

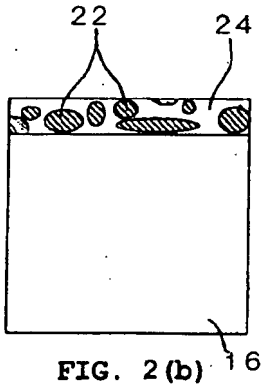

FIG. 2(b)

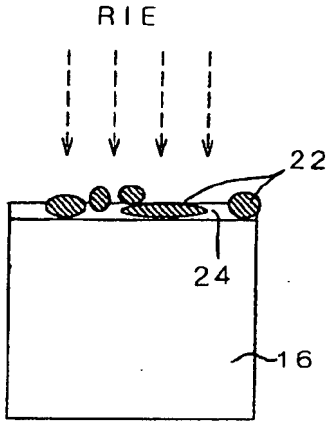

FIG. 2(c)

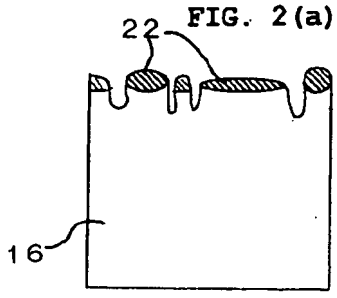

FIG. 2(d)

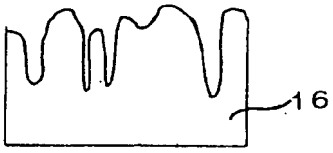

FIG. 2(e)

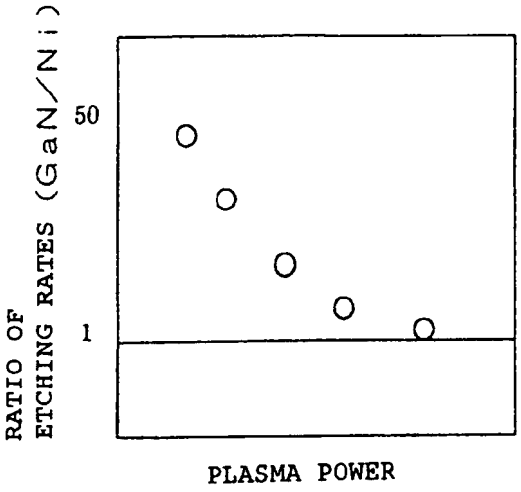
RATIO OF ETCHING RATES (GaN/Ni)
50
1
PLASMA POWER

FIG. 3(a)

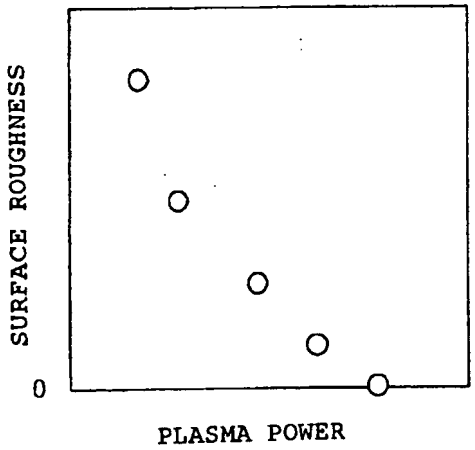
SURFACE ROUGHNESS
0
PLASMA POWER

FIG. 3(b)

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 02 10 0242

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X	EP 0 731 490 A (EBARA CO) 11 September 1996 (1996-09-11) * column 5, line 5 - column 6, line 51 *	1	H01L33/00 H01L21/308 H01L21/033
A	US 3 909 929 A (DEBESIS J) 7 October 1975 (1975-10-07) * column 2, line 39 - column 3, line 7 *	1-3	
A	EP 0 180 222 A (FUJI ELECTRIC CO) 7 May 1986 (1986-05-07) * page 4 *	1	

TECHNICAL FIELDS SEARCHED (Int.Cl.7)

H01L
B41N

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	19 December 2002	van der Linden, J.E.

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 02 10 0242

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

19-12-2002

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 0731490 A	11-09-1996	JP 3069504 B2	24-07-2000
		JP 8238426 A	17-09-1996
		JP 3022948 B2	21-03-2000
		JP 8241884 A	17-09-1996
		JP 8238580 A	17-09-1996
		EP 0731490 A2	11-09-1996
		US 6048671 A	11-04-2000
		US 6010831 A	04-01-2000
		US 6007969 A	28-12-1999
		US 5894058 A	13-04-1999
		DE 69615721 D1	15-11-2001
		DE 69615721 T2	08-08-2002
		EP 0732624 A2	18-09-1996
		JP 8318386 A	03-12-1996
		JP 8318387 A	03-12-1996
		JP 8318378 A	03-12-1996
		US 6015976 A	18-01-2000
		US 5868952 A	09-02-1999
US 3909929 A	07-10-1975	DE 2461210 A1	10-07-1975
		JP 50098796 A	06-08-1975
EP 0180222 A	07-05-1986	JP 1747498 C	25-03-1993
		JP 4036586 B	16-06-1992
		JP 61108176 A	26-05-1986
		DE 3584071 D1	17-10-1991
		EP 0180222 A2	07-05-1986
		US 4664748 A	12-05-1987

EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82